We claim

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1. A global positioning system (GPS) receiver, comprising:

a converter for converting received GPS signals to in-phase (I) and quadrature-phase (Q) digital signals;

a correlator for generating expected codes and correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values for a tap;

a filter for filtering the sampled I values and sampled Q values to modified I values to each of the modified Q values, and for adding each of the modified I values to each of the corresponding modified Q values of the tap, and for outputting a count for sum which is positive;

a counter for incrementing a counter value upon each count received from the filter; and

a comparator for comparing the counter value to a threshold value upon completion of measure of values of the tap for determining the presence of a peak.

2. The receiver of claim 1, wherein the sampled I values and sampled Q values are modified by assigning a positive value to the sampled I value or sampled Q value when a present sample I value or Q value has a different sign from the immediately prior sample I value or sample Q value.

3. The receiver of claim 1, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

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- 4. The receiver of claim 3, wherein the fractional reduction is one half.
- 5. The receiver of claim 1, further including a memory for storing sampled I and Q values of the tap found to have a counter value exceeding the threshold, wherein sampled I and Q values of other taps are not stored in the memory.
- 6. The receiver of claim 5, further including a domain transformer for performing domain transform on data stored in the memory.
- 7. The receiver of claim 1, wherein the filter includes a pair of delay elements and a pair of single bit comparators, wherein the delay elements delay a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and the single bit comparators compare a sign of the present sampled Q value with the prior sign value to provide a positive output if the present and the prior sign values are different.

- 8. The receiver of claims 1, wherein the memory is one of a SRAM or a DRAM.
- 9. A global positioning system (GPS) receiver, comprising:

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a converter for converting received GPS signals to in-phase (I) and quadrature-phase (Q) digital signals;

a correlator for generating expected codes and correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values for a tap;

a filter for filtering the sampled I values and sampled Q values to modified I values and modified Q values, and for adding each of the modified I values to each of the corresponding modified Q values of the tap, and for outputting a count for each sum which is positive;

a counter for incrementing a counter value upon each count received from the filter:

a comparator for comparing the counter value to a threshold value upon completion of measure of values of the tap for determining the presence of a peak; and

a memory for storing the sum of each of the modified I values and corresponding modified Q values of the tap having a counter value exceeding the threshold.

10. The receiver of claim 9, wherein the sampled I values and sampled Q

values are modified by assigning a positive value to the sampled I value or sampled Q value when a present sample I value or Q value has a different sign from the immediately prior sample I value or sample Q value.

- The receiver of claim 9, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.
- 12. The receiver of claim 11, wherein the fractional reduction is one half.
 - 13. The receiver of claim 9, further including a domain transformer for performing domain transform on data stored in the memory.
- 15 14. The receiver of claim 13, wherein the domain transformer is a Fast Fourier Transformer.
 - 15. The receiver of claim 9, wherein the filter includes a pair of delay elements and a pair of single bit comparators, wherein the delay elements delay a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and the single bit comparators compare a sign of the present sampled Q value with the prior sign value to provide a negative output if the present and the prior sign values are different.

- 16. The receiver of claim 9, wherein the memory further stores the sampled I and Q values of the tap identified as having a peak.
- 17. The receiver of claim 9, wherein the memory is one of a SRAM or a DRAM.
- 18. A method of processing global positioning system (GPS) signals for determining position, comprising:

converting received GPS signals to in-phase (I) and quadrature-phase (Q) digital signals;

correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values for a tap;

filtering the sampled I values and sampled Q values to modified I values and modified Q values, adding each of the modified I values to each of the corresponding modified Q values of the tap, and outputting a count for each sum which is positive;

incrementing a counter value upon each count received from the filter; and comparing the counter value to a threshold value upon completion of measure of values of the tap for determining the presence of a peak.

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19. The receiver of claim 18, wherein the sampled I values and sampled Q values are modified by assigning a positive value to the sampled I value or sampled Q value when a present sampled I value or Q value has a different sign

from the immediately prior sampled I value or sampled Q value.

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- 20. The method of claim 18, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.
- 21. The method of claim 18, wherein the fractional reduction is one half.
- 10 22. The method of claim 18, further including storing in a memory sampled I and Q values of the tap having a counter value exceeding the threshold, wherein sampled I and Q values of other taps are not stored in the memory.
 - 23. The method of claim 22, wherein the memory is one of a SRAM or a DRAM.
 - 24. The method of claim 22, further including performing domain transform on data stored in the memory.
- 25. The method of claim 18, further including storing the sum of each of the modified I values and corresponding modified Q values of the tap found to have a counter value exceeding the threshold.

- 26. The method of claim 25, wherein the memory is one of a SRAM or a DRAM.
- 27. The method of claim 25, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

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- 28. The method of claim 27, wherein the fractional reduction is one half.
- 29. The method of claim 25, further including storing in the memory the sampled I and Q values of the tap found to have a peak, wherein sampled I and Q values of taps not found to have a peak are not stored in the memory.
- 15 30. The method of claim 29, further including performing domain transform on data stored in the memory.
 - 31. The method of claim 30, wherein the domain transform is Fast Fourier Transform.
 - 32. The method of claim 29, wherein the memory is one of a SRAM or a DRAM.

33. A stored program device having stored codes executable by a processor to perform method steps for processing GPS signals, the method comprising:

correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values for a tap;

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filtering the sampled I values and sampled Q values to modified I values and modified Q values, adding each of the modified I values to each of the corresponding modified Q values of the tap, and outputting a count for each sum which is positive;

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incrementing a counter value upon each count received from the filter; and comparing the counter value to a threshold value upon completion of measure of values of the tap for determining the presence of a peak.

- 34. The receiver of claim 33, wherein the sampled I values and sampled Q values are modified by assigning a positive value to the sampled I value or sampled Q value when a present sampled I value or Q value has a different sign from the immediately prior sampled I value or sampled Q value.
- 35. The method of claim 33, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.
- 36. The method of claim 33, further including storing in a memory sampled I

and Q values of the tap having a counter value exceeding the threshold, wherein sampled I and Q values of other taps are not stored in the memory.

- 37. The method of claim 33, further including performing domain transform on data stored in the memory.
 - 38. The method of claim 33, further including storing the sum of each of the modified I values and corresponding modified Q values of the tap found to have a counter value exceeding the threshold.

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39. The method of claim 38, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

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40. The method of claim 33, further including storing in the memory the sampled I and Q values of the tap found to have a peak, wherein sampled I and Q values of taps not found to have a peak are not stored in the memory.

- 41. The method of claim 38, further including performing domain transform on data stored in the memory.
- 42. The method of claim 38, wherein the memory is one of a SRAM or a

DRAM.

43. The stored program device of claim 33, wherein the stored program device is one of a flash memory or ROM.